N-Type, Ion-Implanted Silicon Solar Cells and Modules

Daniel L. Meier, *Member, IEEE*, Vinodh Chandrasekaran, *Member, IEEE*, H. Preston Davis, Adam M. Payne, *Member, IEEE*, Xiaoyan Wang, *Member, IEEE*, Vijay Yelundur, Jon E. O'Neill, Young-Woo Ok, Francesco Zimbardi, and Ajeet Rohatgi, *Fellow, IEEE*

***Abstract*—Ion-implanted, screen-printed, high-efficiency, stable, n-base silicon solar cells fabricated from readily available 156-mm pseudosquare Czochralski wafers are described, along with prototype modules assembled from such cells. Two approaches are presented. The first approach, which involves a single phosphorus implant, has been used to produce cells (239 cm^2) having a tight distribution of J_{sc}, V_{oc}, and fill factor over a wide range of wafer resistivity (factor of 10), with Fraunhofer-certified efficiencies up to 18.5%. In spite of the full screen-printed and alloyed Al back, a method has been developed to solder such cells in a module. The second approach, which involves implanting both phosphorus for back-surface field (BSF) and boron for front emitter, has been used to produce n-base cells having local back contacts and dielectric (SiN_x/SiO_2) surface passivation. Efficiencies up to 19.1%, certified by Fraunhofer, have been realized on 239-cm^2 cells. A method is also presented to express recombination activity in the cell base as a component of total reverse saturation current density. This allows recombination activity in all three regions of the cell (n^+ region and its surface, n-base, and p^+ region and its surface) to be compared as components of the total cell J_0 to aid in maximizing V_{oc}.**

***Index Terms*—High efficiency, ion implantation, silicon, solar cell.**

I. Introduction

ALL MONOCRYSTALLINE silicon solar cells based on B-doped Czochralski (Cz) wafers, which have oxygen concentrations up to 1E+18 O/cm^3, suffer from light-induced degradation (LID) associated with a boron–oxygen complex [1]. LID reduces the power output from modules by 1–3% (relative) after they are exposed to sunlight in the field for several days. Effectively, LID reduces the cell efficiency by 0.2–0.5% (absolute). In addition, the lifetime of minority carrier electrons in p-base cells is sensitive to common chemical defects (e.g., Fe) and structural defects (e.g., dislocations) so that it is difficult to achieve and maintain high lifetime through cell processing in p-base wafers. Iron, in particular, is ubiquitous in the cell-processing environment (stainless steel components) and will begin to introduce instability in p-base cells at the extremely low concentration of 1E+10 Fe_i/cm^3. This was observed by in-house measurements of local internal quantum efficiency which were correlated with local Fe concentration as determined by the surface photovoltage mapping technique [2]. Instability follows from the formation of the Fe-B defect in the dark at room temperature and its subsequent dissociation, where Fe goes to an interstitial site under illumination >0.1 sun [3], [4]. Instability increases as Fe concentration increases in B-doped Cz wafers and becomes quite significant at 1E+12 Fe_i/cm^3 (from in-house measurements).

To enable higher efficiencies and to avoid LID and Fe-related instability, cell structures based on n-type Cz-grown wafers can be considered. Such wafers are free from LID (no B to form B–O defect) and from Fe-related instability (no B to form Fe–B defect), have high lifetime in the starting wafer (typically >1 ms), and can preserve this high lifetime through high-temperature processes (up to 1000 °C).

The key new processing technique to be employed in the high-efficiency cell structures described in this paper is ion implantation of P and B. Ion implantation is in common use throughout integrated circuit processing because of its high degree of dose uniformity (<2%), chemical purity of the beam (mass analyzed), and controlled depth of implant (ion energy).

Ion implantation has also been used to produce monocrystalline silicon solar cells. Early implanted cells had an efficiency of 15.0% [5], advancing to 18.0% [6], and then to 19.3% [7] and to 19.5% [8], all laboratory-scale cells of small area (4 cm^2). It is noteworthy that the highest efficiency cells [7], [8] were made with n-type wafers. Interest in ion-implanted emitters and other layers has been reawakened recently [9]. With a throughput of 1000 wafers (156-mm pseudosquare) per hour [10], the cost of the implantation step has been reduced to an acceptable level.

II. Single Implant (P) Process

Fig. 1 shows the structure and processing sequence for a simple n-base cell fabricated from 156-mm pseudosquare n-type Cz wafers that are 200 μm thick. This cell is patterned after the "PhosTop" cell [11], so-named because the top of the cell has a phosphorus-doped front-surface field (FSF). The structure is similar to conventional p-base cells, except the p-n junction is at the rear of the cell, the FSF is selectively doped, and the

Manuscript received July 12, 2011; revised August 27, 2011; accepted September 11, 2011. Date of publication October 25, 2011; date of current version December 27, 2011.

D. L. Meier, V. Chandrasekaran, H. P. Davis, A. M. Payne, X. Wang, V. Yelundur, and J. E. O'Neill are with Suniva, Norcross, GA 30092 USA (e-mail: dmeier@suniva.com; vchandrasekaran@suniva.com; pdavis@suniva.com; apayne@suniva.com; swang@suniva.com; vyelundur@suniva.com; joneill@suniva.com).

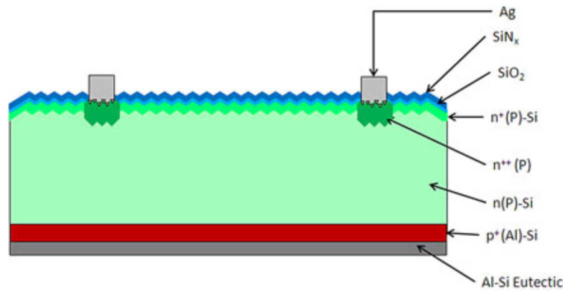
Y.-W. Ok and F. Zimbardi are with the University Center of Excellence for Photovoltaics, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: yok6@mail.gatech.edu; Francesco@gatech.edu).

A. Rohatgi is with Suniva, Norcross, GA 30092 USA, and also with the University Center of Excellence for Photovoltaics, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: ajeet.rohatgi@ece.gatech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JPHOTOV.2011.2169944

2156-3381/$26.00 © 2011 IEEE



Processing Sequence:

1. Etch saw damage and texture (100) wafer surface
2. Implant phosphorus for front surface field
3. Anneal implant damage and grow thermal oxide
4. Deposit SiN$_x$ on front
5. Print/dry back Al contact
6. Print/dry front Ag gridlines
7. Co-fire
8. Apply back soldering pads

Fig. 1. Cell fabricated by the single implant (P) process, with selective FSF, oxide-passivated front surface, and aluminum-alloyed rear p-n junction.

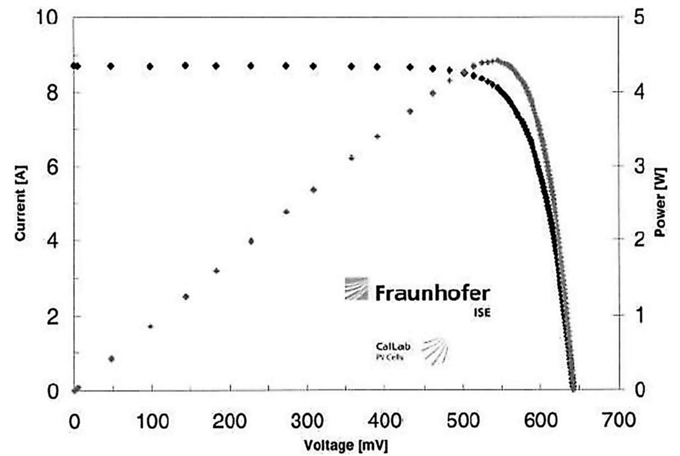


Fig. 2. Fraunhofer-certified full area (239 cm^2) 18.5% Al-alloyed rear emitter cell fabricated from an n-type Cz wafer, with J_{sc} of 36.4 mA/cm^2, V_{oc} of 641 mV, and FF of 0.791.

front surface is passivated with a thermal oxide layer. Apart from removing the saw damage from the starting wafer, the processing sequence is strictly additive and is accomplished in just eight steps, as noted. This is one step fewer than needed for typical $POCl_3$-diffused p-base cells, as the subtractive steps of removing the phosphosilicate glass and laser edge isolation are eliminated. The selective phosphorus FSF is formed by a masked implant [10] along with a thermal anneal of implant damage. The masked implant is accomplished by first exposing the full wafer area to the ion beam (no mask) to implant the lightly doped field region and then inserting a mask with slotted openings over the wafer to implant the heavily doped contact region. The front SiO_2 passivation layer is obtained as a no-cost byproduct of the anneal. A selective FSF is optional, as a uniform FSF also performs well with no need for alignment of grid lines to selectively implanted regions. Al and Ag contacts are screen printed, and all process steps of Fig. 1 have been demonstrated.

Fig. 2 shows a certified efficiency of 18.5% for a full-sized (156-mm pseudosquare) cell having the structure shown in Fig. 1 except for the back soldering pads. A typical acceptor dopant profile for the p$^+$ rear emitter is given in Fig. 3, as obtained by the electrochemical capacitance–voltage (ECV) technique after the Al layer was removed by etching in HCl. Note a maximum doping concentration of 2E+19 acceptors/cm^3 and a junction depth of 4.1 μm, resulting in a measured sheet resistance of the p$^+$ layer of about 20 Ω/square. This maximum doping concentration is about an order of magnitude higher than that typically measured for an Al-alloyed region and suggests that the Al dopant may be supplemented with B dopant incorporated (in a proprietary fashion) by the paste manufacturer, perhaps via a B glass frit [12], [13], [30]. A typical P dopant profile for the n^{++} region beneath the front contact in the selective FSF structure is given in Fig. 4. Here, the maximum doping concentration is 2E+20 P/cm^3 with a junction depth of 0.6 μm, giving a measured sheet resistance of about 50 Ω/square.

It has been found that Al-alloyed rear emitter cells can be made with high yield and quite uniform properties, even with

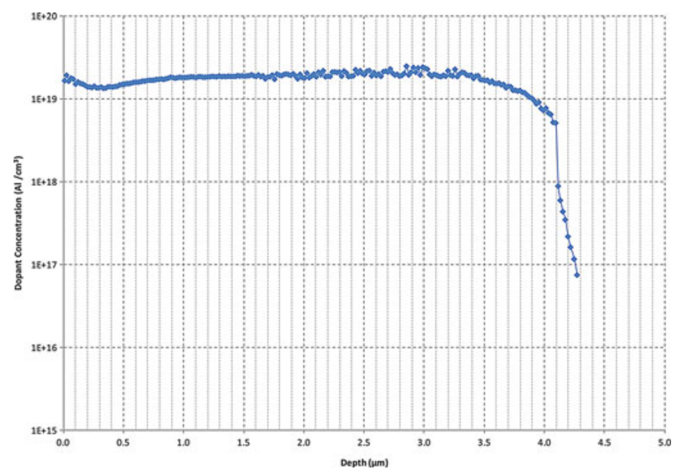


Fig. 3. Typical rear acceptor doping profile for the n$^+$np$^+$ cell fabricated by the single implant (P) process, as measured by the ECV technique.

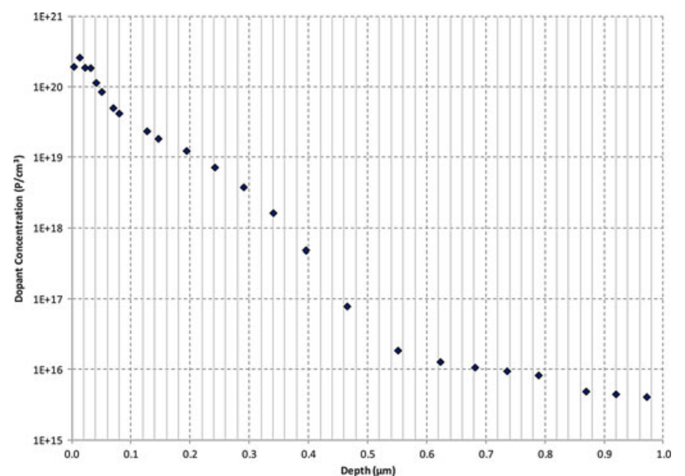


Fig. 4. Typical front phosphorus doping profile for the n$^+$np$^+$ cell fabricated by the single implant (P) process, as measured by the ECV technique. Profile was measured for the more heavily doped n^{++} region beneath the front contacts of the selective FSF region.

TABLE I
AL-ALLOYED REAR EMITTER CELLS (239 cm^2) WITH UNIFORM FSF SHOWING TIGHT DISTRIBUTION AND 18.4% AVERAGE EFFICIENCY

Sample ID	I_{sc} (A)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	Efficiency (%)
242	8.69	36.4	634	0.795	18.3
243	8.68	36.3	635	0.797	18.4
244	8.68	36.3	636	0.797	18.4
245	8.69	36.4	635	0.794	18.4
246	8.70	36.4	634	0.794	18.4
247	8.72	36.5	635	0.795	18.4
250	8.69	36.4	635	0.796	18.4
Average	**8.70**	**36.4**	**635**	**0.796**	**18.4**

starting wafer resistivity ranging over a factor of 10. An example is given in Table I (note uniform rather than selective FSF). The doping profile for such a uniform FSF is given in Fig. 4. These cells typically have high dark shunt resistance (>100 Ω) and low leakage current at −10 V bias (<0.04 A). Note that the cell efficiency for a selective FSF (see Fig. 2) is only marginally better (0.1%) than that for a uniform FSF (see Table I). Quantum efficiency measurements for the selective FSF cells generally show a somewhat better blue response than do cells with a uniform FSF. However, this gain is nearly offset by a reduced fill factor (FF) associated with the higher series resistance from the more lightly doped field region for selective FSF cells. For sake of comparison, a similar screen-printed n-base Cz silicon cell with rear aluminum emitter and selective FSF formed by a structured $POCl_3$ diffusion source (rather than P implant) has been reported at 17.6% [14].

Although laboratory-scale cells (4 cm^2) with Al-alloyed rear emitters have reached 20.0% with amorphous Si passivation of the p^+ emitter surface [15] and 20.1% with Al_2O_3 passivation [16], it is believed that the cell in Fig. 2 represents the highest efficiency achieved for production-worthy cells (239 cm^2), where the alloyed Al remains in contact with the p^+ emitter and where the front contacts are screen printed. Similar results for large-area cells have been reported recently with somewhat different processing conditions (plated contacts, planarized back) [17], [18]. Furthermore, detailed modeling of this cell structure suggests efficiencies in the neighborhood of 19.5% are possible with advanced metallization [19]. In fact, large-area cells have been reported at 19.3% [17] and 19.4% [20] for 100% rear Al coverage. Such complete coverage was achieved by removing 1-mm-wide strips from the edges of the original cell. These strips were not covered by Al paste and, hence, had little or no emitter within this 1-mm border.

III. PROTOTYPE MODULES

Cells with an Al-alloyed rear emitter, as shown in Fig. 1, present a challenge for conventional module assembly, since the Al surface is not solderable. In the more common p-base cell structure, two or three Ag stripes can be screen printed directly onto the rear Si surface to serve as soldering pads, with the screen-printed Al then overlapping the Ag pads along their edges. This method will not work with the n-base cell, since the presence of the Ag soldering pads in direct contact with the Si precludes the formation of a p^+ emitter region beneath them.

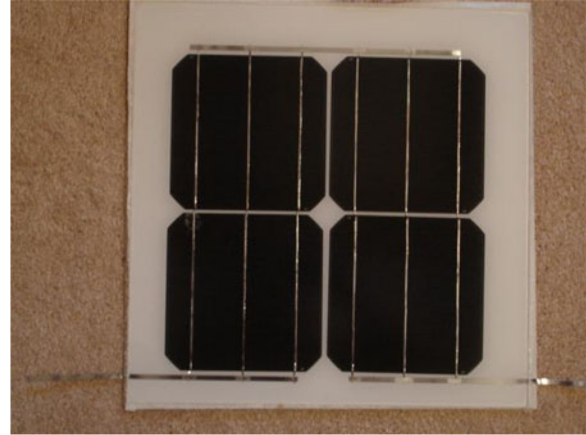


Fig. 5. Minimodule with soldered Al-alloyed rear emitter cells.

The Ag pads then effectively shunt the p^+ emitter to the n-base. Several approaches to overcome this difficulty have been reported. These include local mechanical abrasion of the Al layer down to the p^+ Si surface and the subsequent screen printing of an AgAl paste in the abraded region [21], use of a screen-printed "peeling paste" to lift off the Al where desired [22], and the incorporation of a commercially available conductive film along with selective abrasion [23]. In the work reported here, a method based on the deposition of three Cu soldering pads, which are applied as stripes directly to the back Al, has been developed. Two Cu deposition methods were employed, i.e., sputtering and a plasma source, and both gave equivalent results. These soldering pads are not shown explicitly in the cross-sectional view of Fig. 1 because they run perpendicular to the Ag grid lines, and the section chosen for the drawing does not intersect the soldering pads.

A four-cell minimodule made in this manner with Al-alloyed rear emitter cells is shown in Fig. 5. Cells were interconnected by soldering, with a module FF of 0.755 as-fabricated. The minimodule was subjected to thermal cycles (−40 °C to +85 °C) per IEC 61215 to test the interconnect system. It survived more than the 200 cycles that are required by IEC with no degradation in power output, as shown in Fig. 6. Minimodule power prorated to a standard 60-cell module is 250 W after 216 thermal cycles. The minimodule was also subjected to outdoor sun exposure for a total of 44 h, again without degradation (no LID), as expected for stable n-type cells. Three other four-cell minimodules have also completed the thermal cycling test, with no degradation after 200 thermal cycles.

IV. ANALYSIS OF CELL WITH SINGLE IMPLANT PROCESS

A key analysis tool in assessing performance limitations in silicon solar cells is the quasi-steady-state photoconductivity decay (QSSPCD) measurement [24] of symmetric test structures (e.g., $SiN_x/SiO_2/n^+nn^+/SiO_2/SiN_x$), with the n-region driven into high-level injection (HLI). This technique allows the separation of recombination activity into the front n^+ region and its surface (J_{0n+}), the bulk n region (J_{0n}), and the back p^+ region and its surface (J_{0p+}). Seminal work has been done using

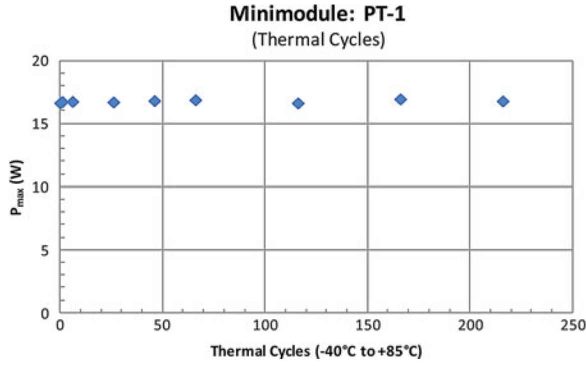


Fig. 6. No degradation in $P_{\max}$ after 216 thermal cycles ($-40\,°$C to $+85\,°$C), showing a stable interconnect system.

transient photoconductivity decay (PCD) to assess recombination in phosphorus-diffused layers having thermally oxidized surfaces [25] and in boron-diffused layers having thermally oxidized surfaces [26] to provide some idea of values to expect.

The PCD method was first described in [27]. The key concept is that recombination activity within the bulk of the wafer (characterized by excess carrier lifetime τ) can be separated from recombination activity within the thin heavily doped "emitter" region along with its surface (characterized by reverse saturation current density component J_{0e}), provided the bulk of the wafer can be driven into HLI, while the emitter region remains in low-level injection (LLI). HLI is defined as the condition where the concentration of minority carriers significantly (factor of 10 or more) exceeds the net doping concentration, while LLI is defined as the condition where the concentration of minority carriers is significantly less than the net doping concentration. In the PCD method, excess carriers (electrons and holes) are created in equal numbers by the absorption of light. For the bulk of the wafer to reach HLI, the light intensity must be sufficiently great and the lifetime of excess carriers must be sufficiently long. In practice, this is achieved by using high-quality wafers (i.e., float zone (FZ) or Cz) that are lightly doped (>10 Ω·cm, or <4.5E+14 cm^{-3} for n-type). Emitter doping is typically >1E+19 cm^{-3}, and Auger recombination keeps lifetime low; therefore, the emitter remains in LLI. The system under test then consists of the wafer bulk and its near-surface layers.

Kane *et al*. [27, eq. (6)] give the recombination current density for the structure considered there ($SiO_2/p^+n/SiO_2$) as

$$J_{\text{rec,total}} = -qW\left(\frac{d\Delta n}{dt}\right) = qW\left(\frac{\Delta n}{\tau_{\text{hli}}}\right) + q(\Delta n)s + J_{0E}(\Delta n/n_i)^2 \quad (1)$$

where Δn is the excess carrier density (i.e., carriers in excess of the equilibrium density), τ_{hli} is the lifetime of the excess carriers in the wafer bulk under HLI conditions, J_{0E} is the component of the reverse saturation current density associated with the front heavily doped "emitter" and its surface, s is the surface recombination velocity of the rear oxidized surface, q is the electronic charge, W is the width (thickness) of the wafer bulk, and n_i is the intrinsic carrier concentration.

A typical cell structure has a p-n junction on one side and a high–low junction on the other. For example, a rear p-n junction structure can be considered with oxide-passivated surfaces and a high–low FSF to give $SiO_2/n^+np^+/SiO_2$. In this case, (1) can be rewritten as

$$J_{\text{rec,total}} = J_{0n+}\left(\frac{\Delta n}{n_i}\right)^2 + qW\left(\frac{\Delta n}{\tau_{\text{hli}}}\right) + J_{0p+}\left(\frac{\Delta n}{n_i}\right)^2 \quad (2)$$

where recombination in the front n^+ layer and its surface is represented by $J_{0\text{n}+}$, and recombination in the rear p^+ layer and its surface is represented by $J_{0\text{p}+}$. It would be convenient if recombination in the central n-type layer (bulk) could also be expressed in the form of a reverse saturation current density $J_{0\text{n}}$ so that recombination activity in the three regions could be compared on a common footing. This can be accomplished by defining $J_{0\text{n}}$ as follows:

$$qW\left(\frac{\Delta n}{\tau_{\text{hli}}}\right) \equiv J_{0n}\left(\frac{\Delta n}{n_i}\right)^2 \quad (3)$$

to be consistent with the other J_0 terms in (2). Thus

$$J_{0n} \equiv \left[\frac{qWn_i^2}{\tau_{\text{hli}}}\right] * \left[\frac{1}{\Delta n}\right]. \quad (4)$$

Now, the excess carrier concentration Δn can be expressed in terms of the generation rate G of electron–hole (e–h) pairs within the wafer bulk and the lifetime of these carriers under HLI conditions (τ_{hli}) as

$$\Delta n = G * \tau_{\text{hli}}. \quad (5)$$

Here, G, in turn, can be expressed in terms of the flux of photons with sufficient energy to generate an e–h pair (Φ) and the thickness of the bulk region (W) as

$$G = \frac{\Phi}{W}. \quad (6)$$

Thus, from (5) and (6), Δn can be expressed as

$$\Delta n = \left(\frac{\Phi}{W}\right) * \tau_{\text{hli}}. \quad (7)$$

Substituting (7) into (4) gives

$$J_{0n} \equiv \left[\frac{qW^2n_i^2}{\Phi}\right] * \left[\frac{1}{\tau_{\text{hli}}^2}\right]. \quad (8)$$

Equation (8) shows that $J_{0\text{n}}$ varies inversely with the square of τ_{hli}. Note that wafer doping density does not appear in the expression for $J_{0\text{n}}$ in (8). This is because doping density is not relevant for HLI conditions.

The photon flux Φ can be estimated from $J_{0\text{-}\lambda}$, the cumulative current density available up to wavelength λ for the AM1.5 Global spectrum at 100 mW/cm^2, as given in [28]. Taking the current up to a wavelength of 1.107 μm (corresponding to the Si bandgap of 1.120 eV) gives 43.12 mA/cm^2. This allows a determination of Φ as

$$\Phi = \frac{J_{0\text{-}\lambda}}{q} \quad (9)$$

TABLE II
CALCULATED J_{0n} AS A FUNCTION OF τ_{hli} ACCORDING TO (11)

τ_{hli} (μs)	J_{0n} (fA/cm^2)
100	2,260
200	566
400	142
600	63
800	35
1000	23
2000	6

where q is the charge on the electron (1.602E-19 C). Thus, $\Phi = 2.692\text{E+}17$ photons/cm^2-s. Typically, there is some loss of photons at the illuminated surface of the wafer by reflection R; therefore, the flux of photons responsible for generating e–h pairs in the Si is somewhat less than Φ and is given by $(1 - R)*\Phi$. Substituting this refinement into (8) gives

$$J_{0n} \equiv \left[\frac{qW^2 n_i^2}{(1-R)\Phi}\right] * \left[\frac{1}{\tau_{\text{hli}}^2}\right]. \quad (10)$$

For a textured monocrystalline Si surface with an SiN_x/SiO_2 dielectric antireflective stack, R (average reflectivity weighted by AM1.5 Global spectrum) has been measured (in-house) to be 0.025. The width of the base (bulk) in a typical finished cell after etching to remove saw damage is 0.0180 cm for W. The remaining constants are 1.602E-19 C for q, 1.07E+10/cm^3 for n_i [29], and 2.692E+17/cm^2-s for Φ. With these values, (10) becomes

$$J_{0n} \equiv 2.264\text{E-}20(A - s^2/\text{cm}^2) * \left[\frac{1}{\tau_{\text{hli}}^2}\right]. \quad (11)$$

For example, if τ_{hli} is 1 ms, $J_{0\text{n}}$ is 23 fA/cm^2. Calculated $J_{0\text{n}}$ values are given for various values of τ_{hli} in Table II. Note that τ_{hli} should be at least 400 μs to obtain a reasonably good $J_{0\text{n}}$ value (142 fA/cm^2), and for τ_{hli} above 2 ms, $J_{0\text{n}}$ is negligible.

Thus, a cell can be divided into three distinct regions: front heavily doped region and its surface, rear heavily doped region and its surface, and the region between (bulk). By using symmetric test structures (e.g., $SiN_x/SiO_2/n^+nn^+/SiO_2/SiN_x$) and wafers with high lifetime, QSSPCD measurements can be made to extract a τ_{hli} and a $J_{0\text{n}+}$ value at various stages of processing. This lifetime value can be transformed into a reverse saturation current density for comparison with those values for the heavily doped regions. This allows a means to assess which of the three cell regions must be improved in order to increase V_{oc}.

As a check of the validity of this approach, the V_{oc} value that is calculated from the expression $V_{\text{oc}} = V_T*\ln(J_{\text{sc}}/J_0)$ was compared with the implied V_{oc} value obtained from the QSSPCD measurement of a symmetric test structure ($SiN_x/SiO_2/p^+np^+/SiO_2/SiN_x$) after simulated firing (no metals). The starting n-type wafer had resistivity above 10 Ω·cm to enable HLI conditions. The p$^+$ region was formed by ion implantation of B followed by a thermal anneal to create the oxidized p$^+$ layer, and SiN_x was deposited by plasma-enhanced chemical vapor deposition (PECVD). For the calculated V_{oc} value, $J_{0\text{n}}$ was first determined from (11) using the τ_{hli} value measured by QSSPCD (intercept) and $J_{0\text{p}+}$ was also obtained

TABLE III
COMPARISON OF THE CALCULATED V_{oc} WITH THE IMPLIED V_{oc} FOR SYMMETRIC TEST STRUCTURES ($SiN_x/SiO_2/p^+np^+/SiO_2/SiN_x$) WHICH WERE PROCESSED UNDER DIFFERENT CONDITIONS, ALL AFTER SIMULATED FIRING (NO METALS), SHOWING GOOD AGREEMENT

J_{0p+} (fA/cm^2)	τ_{hli} (μs)	Imp V_{oc} (mV)	J_{0n} (fA/cm^2)	J_{0p+np+} (fA/cm^2)	Calc V_{oc} (mV)	ΔV_{oc} (mV)
120	100	613	2260	2500	602	-11
124	268	637	315	563	641	+4
410	62	584	5890	6710	577	-7
377	360	617	175	929	628	+11
1210	95	579	2510	4930	585	+6
644	284	603	281	1570	614	+11

from the QSSPCD measurement (slope). J_0 was then calculated as twice $J_{0\text{p}+}$ plus $J_{0\text{n}}$ ($J_{0\text{p}+\text{np}+}$), V_T was taken to be 25.7 mV (appropriate for 25 °C), and J_{sc} was assumed to be 37.6 mA/cm^2. Results for six samples are given in Table III. The average difference between the calculated V_{oc} and implied V_{oc} is (2 ± 9 mV). This reasonably good agreement supports the validity of converting τ_{hli} into $J_{0\text{n}}$, a reverse saturation current density component, to aid in the cell analysis.

The total J_0 for the entire Al-alloyed rear emitter cell is known from the expression $J_0 = J_{\text{sc}}*\exp(-V_{\text{oc}}/V_T) = 536$ fA/cm^2 with J_{sc} and V_{oc} of Fig. 2 and V_T of 25.7 mV. $J_{0\text{n}+}$ was determined from the slope of the QSSPCD curve to be 40 fA/cm^2 for a typical selective FSF with its metallized (Ag grid) surface. $J_{0\text{n}}$ was determined from the intercept of the QSSPCD curve (gives τ_{hli} of 448 μs) to be 113 fA/cm^2. This is determined from (11).

It then follows that the Al-doped emitter has a J_0 component of $J_{0\text{p}+} = (536 - 40 - 113)$ fA/cm^2 $= 383$ fA/cm^2. This value falls within the range of 370–490 fA/cm^2 given in [30] for a p$^+$ sheet resistance of 20 Ω/square, i.e., the value measured in this study. It is desirable to reduce this value of $J_{0\text{p}+}$ in order to increase cell V_{oc}.

V. DOUBLE IMPLANT (B, P) PROCESS

The rather high value of $J_{0\text{p}+}$ (383 fA/cm^2), associated with the fully metallized Al-alloyed rear emitter as described previously, along with the poor reflectivity at the back Si surface, limit cell efficiency. These factors are addressed by a double implant process. The resulting structure, which is shown in Fig. 7, employs a front-side B emitter, local back contacts to reduce $J_{0\text{n}+}$ and a dielectric passivation of the back surface to increase reflectivity. The process sequence for this cell is more complicated than that of Fig. 1, in that two implants, two anneals (B requires a higher anneal temperature than does P), and two SiN_x depositions are required. Full-sized, 156-mm pseudosquare n-type commercially available Cz wafers, which are 200 μm thick, were used. After conventional texturing using KOH and IPA, the B-doped emitter was formed by implantation and thermal annealing. A P-doped BSF was also created by thermal annealing after P implantation. Both front and back surfaces of this cell were passivated by a stack of thermal SiO_2 grown during implant annealing and PECVD SiN_x layers. Printing and firing through the stack were carried out to make ohmic contacts. A Fraunhofer-certified efficiency of 19.1% is shown in Fig. 8, with J_{sc} of 38.4 mA/cm^2, V_{oc} of 644 mV, and FF of

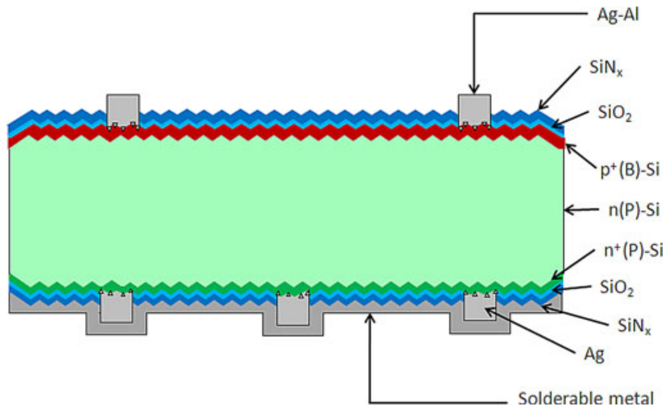


Fig. 7. Structure of B-front emitter n-type cell fabricated by the double implant (B, P) process.

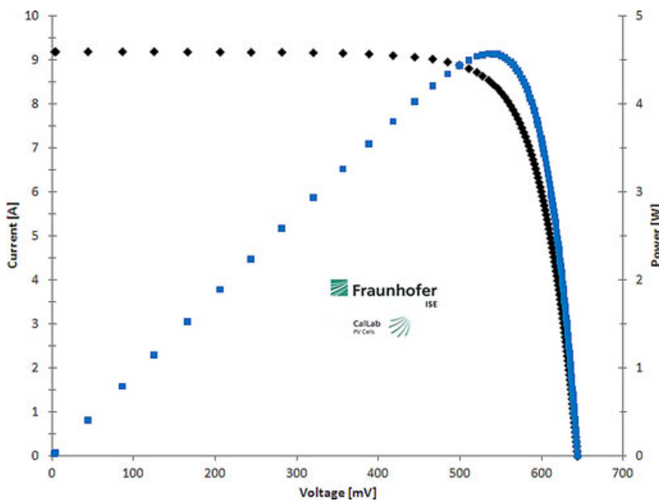


Fig. 8. Certified 19.1% full-area (239-cm^2, n-Cz wafer) n-base cell with implanted B-emitter and implanted P-BSF.

0.773. The high J_{sc}, even with 8% grid shadowing, is attributed to good base lifetime in the finished cell and to high reflectivity at the back Si surface. The relatively high V_{oc} has been obtained by applying SiO_2/SiN_x as a passivation layer to the B-doped emitter. Measured J_{0p+} of the passivated B-doped emitter is 170 fA/cm^2 after simulated firing (without metal).

The 19.1% efficiency obtained here is compared favorably with other results that have been reported recently for large-area, front-junction, n-base cells. These include the PANDA bifacial Cz cell at 18.6% [31], an experimental FZ cell at 18.4% [32], and a bifacial Cz cell at 18.6% [33]. All three of these cells employed a B diffusion (e.g., BBr_3 or BCl_3), while the cell reported here utilized B ion implantation which has the advantage of single-side doping. Still more recently, a large-area (239 cm^2) metal wrap-through n-base cell with a diffused B front emitter has been reported at 19.7% [34], while a fully implanted laboratory scale (4 cm^2) interdigitated back contact n-base cell with a rear B emitter has been reported at 20.0% [35].

VI. Summary

Two types of solar cells that are fabricated from full-sized n-type monocrystalline Cz wafers (156-mm pseudosquare) have been reported. The first is a simple rear junction cell with an alloyed Al emitter which is accomplished with a single implant of P for the FSF. This cell has demonstrated efficiencies up to 18.5%. The second is a front junction cell with B emitter and P-BSF, which is accomplished with a B implant and a P implant, respectively. This cell has exhibited efficiencies up to 19.1%. In both cases, the unmetallized silicon surface is passivated with a thermal oxide which is obtained as a byproduct of the implant anneal step. In addition, a method was presented to assess recombination activity in the base of the cell by casting the measured HLI lifetime in the base as a reverse saturation current density component.

Acknowledgment

The authors would like to thank C. Davis for assembling and testing the minimodules and the Suniva R&D staff for assistance in cell processing and testing.

References

[1] K. Bothe, R. Sinton, and J. Schmidt, "Fundamental boron-oxygen-related carrier lifetime limit in mono- and multicrystalline silicon," in *Progr. Photovoltaics: Res. Appl.*, 2005, vol. 13, pp. 287–296.

[2] J. Lagowski, P. Edelman, A. M. Kontkiewicz, O. Milic, W. Henley, M. Dexter, L. Jastrzebski, and A. M. Hoff, "Iron detection in the part per quadrillion range in silicon using surface photovoltage and photodissociation of iron-boron pairs," *Appl. Phys. Lett.*, vol. 63, pp. 3043–3045, 1993.

[3] D. H. Macdonald, L. J. Geerligs, and A. Azzizi, "Iron detection in crystalline silicon by carrier lifetime measurements for arbitrary injection and doping," *J. Appl. Phys.*, vol. 95, pp. 1021–1028, 2004.

[4] A. A. Istratov, H. Hieslmair, and E. R. Weber, "Iron contamination in silicon technology," *Appl. Phys. A: Mater. Sci. Process.*, vol. 70, pp. 489–534, 2000.

[5] E. C. Douglas and R. V. D'Aiello, "A study of the factors which control the efficiency of ion-implanted silicon solar cells," *IEEE Trans. Electron Devices*, vol. ED-27, no. 4, pp. 792–802, Apr. 1980.

[6] M. B. Spitzer, S. P. Tobin, and C. J. Keavney, "High-efficiency ion-implanted silicon solar cells," *IEEE Trans. Electron Devices*, vol. ED-31, no. 5, pp. 546–550, May 1984.

[7] R. D. Westbrook, R. F. Wood, and G. E. Jellison, Jr., "Glow-discharge-implanted, thermally annealed, oxide-passivated silicon solar cells of 19% efficiency," *Appl. Phys. Lett.*, vol. 50, pp. 469–471, 1987.

[8] R. F. Wood, R. D. Westbrook, and G. E. Jellison, Jr., "Excimer laser-processed oxide-passivated silicon solar cells of 19.5-percent efficiency," *IEEE Electron. Device Lett.*, vol. EDL-8, no. 5, pp. 249–251, May 1987.

[9] T. Janssens, N. Posthuma, B. Pawlak, E. Rosseel, and J. Poortmans, "Implantation for an excellent definition of doping profiles in Si solar cells," in *Proc. 25th Eur. Photovoltaic Sci. Eng. Conf.*, 2010, pp. 1179–1181.

[10] A. Gupta, R. J. Low, N. Bateman, D. Ramappa, H.-J. L. Gossman, Q. Zhai, P. Sullivan, W. Skinner, C. Dubé, B. Tsefrekas, and J. Mullin, "High efficiency selective emitter cells using *in-situ* patterned ion implantation," in *Proc. 25th Eur. Photovoltaic Sci. Eng. Conf.*, 2010, pp. 1158–1162.

[11] D. L. Meier, H. P. Davis, R. A. Garcia, J. Salami, A. Rohatgi, A. Ebong, and P. Doshi, "Aluminum alloy back p-n junction dendritic web silicon solar cell," *Solar Energy Mater. Solar Cells*, vol. 65, pp. 621–627, 2001.

[12] F. Huster and G. Schubert, "ECV doping profile measurements of aluminium alloyed back surface fields," in *Proc. 20th Eur. Photovoltaic Sci. Eng. Conf.*, 2005, pp. 1462–1465.

[13] T. Fellmeth, S. Mack, J. Bartsch, D. Erath, U. Jäger, R. Preu, F. Clement, and D. Biro, "20.1% efficient silicon solar cell with aluminum back surface field," *IEEE Electron Device Letters*, vol. 32, no. 8, pp. 1101–1103, Aug. 2011.

[14] K. Meyer, C. Schmiga, R. Jesswein, M. Dupke, J. Lossen, H.-J. Krokoszinski, M. Hermle, and S. W. Glunz, “All screen-printed industrial n-type Czochralski silicon solar cells with aluminium rear emitter and selective front surface field,” in *Proc. 35th IEEE Photovoltaic Spec. Conf.*, 2010, pp. 3531–3535.

[15] R. Bock, J. Schmidt, S. Mau, B. Hoex, E. Kessels, and R. Brendel, “The ALU^+ concept: n-type silicon solar cells with surface-passivated screen-printed aluminium-alloyed rear emitter,” *IEEE Trans. Electron Devices*, vol. 57, no. 8, pp. 1966–1971, Aug. 2010.

[16] C. Schmiga, M. Hermle, and S. W. Glunz, “Towards 20% efficient n-type silicon solar cells with screen-printed aluminium-alloyed rear emitter,” in *Proc. 23rd Eur. Photovoltaic Sci. Eng. Conf.*, 2008, pp. 982–987.

[17] C. Schmiga, M. Rauer, M. Rüdiger, K. Meyer, J. Lossen, H.-J. Krokoszinski, M. Hermle, and S. W. Glunz, “Aluminum-doped p^+ silicon for rear emitters and back surface fields: Results and potentials of industrial n- and p-type cells,” in *Proc. 25th Eur. Photovoltaic Sci. Eng. Conf.*, 2010, pp. 1163–1168.

[18] S. W. Glunz, J. Benick, D. Biro, M. Bivour, M. Hermle, D. Pysch, M. Rauer, C. Reichel, A. Richter, M. Rüdiger, C. Schmiga, D. Suwito, A. Wolf, and R. Preu, “n-type silicon: Enabling efficiencies >20% in industrial production,” in *Proc. 35th IEEE Photovoltaic Spec. Conf.*, 2010, pp. 50–56.

[19] M. Rudiger, C. Schmiga, M. Rauer, M. Hermle, and S. W. Glunz, “Optimisation of industrial n-type silicon solar cells with aluminum-alloyed rear emitter by means of 2D numerical simulation,” in *Proc. 25th Eur. Photovoltaic Sci. Eng. Conf.*, 2010, pp. 2280–2286.

[20] F. Book, T. Wiedenmann, G. Schubert, H. Plagwitz, and G. Hahn, “Influence of the front surface passivation quality on large area n-type silicon solar cells with Al-alloyed rear emitter,” presented at the 1st SiliconPV Conf., Freiburg, Germany, 2011.

[21] A. Halm, L. M. Popescu, J. Theobald, K. Peter, and R. Kopecek, “Low temperature pads on Al-emitter or Al-BSF,” in *Proc. 24th Eur. Photovoltaic Sci. Eng. Conf.*, 2009, pp. 1462–1464.

[22] T. Pham and W. Zhang, “Improving performance of solar cell by full aluminum back surface field,” in *Proc. 35th IEEE Photovoltaic Spec. Conf.*, 2010, pp. 1019–1022.

[23] R. Kopecek, A. Halm, L. Popescu, K. Peter, and M. A. Vazquez, “Industrial large area n-type solar cells with aluminum rear emitter with stable efficiencies,” in *Proc. 35th IEEE Photovoltaic Spec. Conf.*, 2010, pp. 1423–1426.

[24] R. A. Sinton, A. Cuevas, and M. Stuckings, “Quasi-steady-state photoconductance: A new method for solar cell material and device characterization,” in *Proc. 25th IEEE Photovoltaic Spec. Conf.*, 1996, pp. 457–460.

[25] R. R. King, R. A. Sinton, and R. M. Swanson, “Studies of diffused phosphorus emitters: Saturation current, surface recombination velocity, and quantum efficiency,” *IEEE Trans. Electron Devices*, vol. 37, no. 2, pp. 365–371, Feb. 1990.

[26] R. R. King and R. M. Swanson, “Studies of diffused boron emitters: Saturation current, bandgap narrowing, and surface recombination velocity,” *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1399–1409, Jun. 1991.

[27] D. E. Kane and R. M. Swanson, “Measurement of the emitter saturation current by a contactless photoconductivity decay method,” in *Proc. IEEE Photovoltaic Spec. Conf.*, 1985, pp. 578–583.

[28] M. A. Green, *Silicon Solar Cells, Advanced Principles and Practices.* Sydney, Australia: Centre Photovoltaic Devices Syst., Univ. New South Wales, 1985, App. C.

[29] M. A. Green, “Intrinsic concentration, effective densities of states, and effective mass in silicon,” *J. Appl. Phys.*, vol. 67, pp. 2944–2954, 1990.

[30] R. Woehl, P. Gundel, J. Krause, K. Rühle, F. D. Heinz, M. Rauer, C. Schmiga, M. C. Schubert, W. Warta, and D. Biro, “Evaluating the aluminum-alloyed p^+-layer of silicon solar cells by emitter saturation current density and optical microspectroscopy measurements,” *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 441–447, Feb. 2011.

[31] A. R. Burgers, R. C. G. Naber, A. J. Carr, P. C. Barton, L. J. Geerligs, X. Jingfeng, L. Gaofei, S. Weipeng, A. Haijiao, H. Zhiyan, P. R. Venema, and A. H. G. Vlooswijk, “19% efficient n-type Si solar cells made in pilot production,” in *Proc. 25th Eur. Photovoltaic Sci. Eng. Conf.*, 2010, pp. 106–1109.

[32] Y. Veschetti, V. Sanzone, F. Diagne, N. Auriac, and D. Heslinga, “High efficiency n-type silicon solar cells with novel diffusion technique for emitter formation,” in *Proc. 25th Eur. Photovoltaic Sci. Eng. Conf.*, 2010, pp. 2241–2244.

[33] V. D. Mihailetchi, J. Jourdan, A. Edler, R. Kopecek, R. Harney, D. Stichtenoth, J. Lossen, T. S. Böscke, and H.-J. Krokoszinski, “Screen printed n-type silicon solar cells for industrial application,” in *Proc. 25th Eur. Photovoltaic Sci. Eng. Conf.*, 2010, pp. 1446–1448.

[34] N. Guillevin, B. J. B. Heurtault, L. J. Geerligs, and A. W. Weeber, “Development towards 20% Efficient Si MWT solar cells for low-cost industrial production,” presented at the 1st SiliconPV Conf., Freiburg, Germany, 2011.

[35] N. Bateman, P. Sullivan, C. Reichel, J. Benick, and M. Hermle, “High quality ion implanted boron emitters in an interdigitated back contact solar cell with 20% efficiency,” presented at the 1st SiliconPV Conf., Freiburg, Germany, 2011.

Authors’ photographs and biographies not available at the time of publication.